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09/697,305	10/27/2000	Takaki Yoshida	YMOR:186	4222

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

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15

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/697,305	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) *23-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-7 and 9-22* is/are rejected.

7)☒ Claim(s) *1-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. This application contains claims 23-52 drawn to an invention nonelected with traverse in Paper No. 6. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Response to Arguments

2. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 1-22 are objected to because of the following informalities:

Claim 1 recites the limitation, "corresponding to **at least one of** (a) information identifying locations of a semiconductor integrated circuit where a possible-fault is likely to occur and (b) information required to reduce faults". The Examiner would like to point out that the preface 'at least one of' only requires that one of the limitations be present. Since fault lists generally provide "information required to reduce faults" by providing a mechanism to analyze circuit design so that circuits can be redesigned to reduce faults or by allowing for replacement of faulty circuitry by redundant parts, it is unclear how the previously quoted limitation in claim 1 further limits claim 1. For the purposes of speeding up prosecution on the case the Examiner is assuming the following was

intended: --corresponding to (a) information identifying locations of a semiconductor integrated circuit where a possible-fault is likely to occur and (b) information required to reduce faults--.

Claim 6 should be corrected for grammatical errors.

Claim 12 recites similar language.

Claims 2-11 and 13-22 depend from respective claims 1 and 12; hence inherit the deficiencies in claims 1 and 12.

Appropriate correction is required.

Claims 1-22 are objected to because of the following informalities: the Examiner asserts that independent claims 1 and 12 in the application remain so broad that it is impossible for the Examiner to conclude a thorough search. In the current search, the Examiner reviewed approximately 400 US patents finding various documents that could possibly be used in a rejection of claims 1 and 12, but has not searched any of the European, foreign or Non-patent literature databases because of the overwhelming amount of literature. The Examiner suggests narrowing claims 1 and 12 so that a thorough search can be concluded in order to speed up prosecution on the case.

Claims 2-11 and 13-22 depend from respective claims 1 and 12; hence inherit the deficiencies in claims 1 and 12.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 5, 6, 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 recites, "said fault coverage being a probability of detecting faults in said a semiconductor integrated circuit, and detecting faults using a fault list comprising said weighted possible faults". Note: fault coverage is a probabilistic measure of detecting a set of faults in a semiconductor integrated circuit using a particular fault list; hence the phrase "said fault coverage being a probability of detecting faults in said a semiconductor integrated circuit, and detecting faults using a fault list comprising said weighted possible faults" makes no sense; hence is indefinite. Proper punctuation and indentation is required.

Claims 6, 10 and 11 depend from claims 5; hence inherit the deficiencies in claim 5.

Claims 15 and 18-20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites the limitation "second detecting possible faults" in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claims 18-20 depend from claims 15; hence inherit the deficiencies in claim 15.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran).

35 U.S.C. 102(e) rejection of claim 1.

Balachandran teaches a fault detecting method for a semiconductor integrated circuit (see Abstract in Balachandran; Note: Balachandran teaches that test patterns are applied to an integrated circuit to detect faults used in generating various diagnostic lists), comprising: providing a fault list corresponding to information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur (see Abstract and Figure 2 in Balachandran; Note: Balachandran teaches that a stuck-at-fault dictionary, i.e. a fault list, is provided to the test analysis tool so that the test analysis tool can prune the stuck-at-fault dictionary to construct intermediate and final pruned stuck-at-fault dictionaries referred to as initial diagnostic lists, composite dictionaries and final logical diagnostic list; Note also that Balachandran teaches that the stuck-at-fault dictionary comprises a plurality of nets of the circuit; col.

2, lines 56-60 and col. 6, lines15-20 in Balachandran teach that the system includes a physical database containing physical data for the physical layout of the circuit under test including geographical coordinates corresponding to the nets in the circuit and in particular corresponding to the nets in the stuck-at-fault dictionary, hence Balachandran teaches providing a stuck-at-fault dictionary fault list 100 in Figure 1 of Balachandran containing nets corresponding to information stored in a physical database 70 in Figure 1 identifying geographical coordinates, i.e., physical sites, on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur), and information required to reduce faults (a fault list is information that can be used to reduce faults by providing fault information in the manufacturing or design phase so that corrective actions can be taken, such as; replacing faulty circuitry with redundant circuitry, using error correcting codes, or discarding faulty IC chips during manufacturing, hence a fault list inherently corresponds to information required to reduce faults capable of being used throughout the life-cycle of the integrated circuit); and detecting faults in a semiconductor integrated circuit to which said fault list corresponds, said detecting in accordance with by said fault list (Step 220 in Figure 2 of Balachandran is a step for detecting faults in a semiconductor integrated circuit to which said stuck-at-fault dictionary fault list 100 corresponds, said detecting in accordance with by said stuck-at-fault dictionary fault list 100).

35 U.S.C. 102(e) rejection of claim 3.

The Abstract in Balachandran states that the final logical diagnostic list is ranked in probabilistic order according to the probability of a fault; hence the fault list comprises data about a likelihood of a fault occurring at a physical site.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 2, 4-6, 9, 12-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran) in view of Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh).

35 U.S.C. 103(a) rejection of claim 2.

Balachandran substantially teaches the claimed invention described in claim 1 (as rejected above). In addition, Balachandran teaches omitting possible faults that having a specified low probability of occurrence from the fault list to define a remaining part of the fault list (col. 2, lines 43-48 in Balachandran).

However Balachandran does not explicitly teach the specific use of detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list.

Rohrbaugh, in an analogous art, teaches the typical use of fault lists for compacting test vectors (see Figure 7 in Rohrbaugh). The Examiner asserts that Balachandran teaches a method for creating a pruned fault list, which are typically used and required for designing tests, for creating test pattern sets and for testing for faults in Automatic Test Equipment (ATE) throughout the lifecycle of the DUT. Rohrbaugh, on the other hand teaches a typical use for generating test patterns from a fault list (see Figure 7 in Rohrbaugh) and using generated test patterns for testing a Device Under Test (DUT) by detecting faults using test patterns that were generated using a fault list, hence Rohrbaugh teaches detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Balachandran with the teachings of Rohrbaugh by including an additional step of detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that detecting faults in said

semiconductor integrated circuit by using the remaining part of the fault list would have provided the opportunity to determine the integrity and fault-tolerance of a particular DUT during and after manufacture throughout the lifecycle of the DUT.

35 U.S.C. 103(a) rejection of claim 4.

Balachandran substantially teaches the claimed invention described in claims 1-3 (as rejected above). In addition, Balachandran teaches the final logical diagnostic list is ranked in probabilistic order according to the probability of a fault; hence the fault list comprises data about a likelihood of a fault occurring at a physical site (see Abstract in Balachandran).

However Balachandran does not explicitly teach the specific use of detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list.

Rohrbaugh, in an analogous art, teaches the typical use of fault lists for compacting test vectors (see Figure 7 in Rohrbaugh). The Examiner asserts that Balachandran teaches a method for creating a pruned fault list, which are typically used and required for designing tests, for creating test pattern sets and for testing for faults in Automatic Test Equipment (ATE) throughout the lifecycle of the DUT. Rohrbaugh, on the other hand teaches a typical use for generating test patterns from a fault list (see Figure 7 in Rohrbaugh) and using generated test patterns for testing a Device Under Test (DUT) by detecting faults using test patterns that were generated using a fault list, hence Rohrbaugh teaches detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Balachandran with the teachings of Rohrbaugh by including an additional step of detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list would have provided the opportunity to determine the integrity and fault-tolerance of a particular DUT during and after manufacture throughout the lifecycle of the DUT. Note: fault coverage is a probability of detecting faults in said a semiconductor integrated circuit using a particular fault list.

35 U.S.C. 103(a) rejection of claim 5.

Balachandran substantially teaches the claimed invention described in claims 1-3 (as rejected above). In addition, Balachandran teaches weighting possible faults at physical sites according to their likelihood to achieve a specific fault coverage, thereby creating weighted possible faults (col. 6, lines 31-44 in Balachandran teach that if such a defect can cause a bridging fault between the two particular nets, the determination is weighted using the probability that a defect of that size exists to determine a final probability or ranking that particular bridging fault exists, hence ranking is a means for weighting in the Balachandran patent). Note: fault coverage is a probabilistic measure of detecting a set of faults in a semiconductor integrated circuit using a particular fault

list.

However Balachandran does not explicitly teach the specific use of detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list. Rohrbaugh, in an analogous art, teaches the typical use of fault lists for compacting test vectors (see Figure 7 in Rohrbaugh). The Examiner asserts that Balachandran teaches a method for creating a pruned fault list, which are typically used and required for designing tests, for creating test pattern sets and for testing for faults in Automatic Test Equipment (ATE) throughout the lifecycle of the DUT. Rohrbaugh, on the other hand teaches a typical use for generating test patterns from a fault list (see Figure 7 in Rohrbaugh) and using generated test patterns for testing a Device Under Test (DUT) by detecting faults using test patterns that were generated using a fault list, hence Rohrbaugh teaches detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Balachandran with the teachings of Rohrbaugh by including an additional step of detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list would have provided the opportunity to determine the integrity and fault-tolerance of a particular DUT during and after manufacture throughout the lifecycle of the DUT. Note: fault

coverage is a probability of detecting faults in said a semiconductor integrated circuit using a particular fault list.

35 U.S.C. 103(a) rejection of claim 6.

Col. 5, lines 22-42 in Balachandran teach that a composite dictionary including a listing of faults is used to create the final logical diagnostic list. A listing is an ordered set, i.e., the composite dictionary is ordered; hence Balachandran teaches arranging said possible faults an order in a composite dictionary before weighting said possible faults in the final logical diagnostic list.

35 U.S.C. 103(a) rejection of claim 9.

Defect data arranged in probabilistic order is reliability data giving a clear indication of the reliability of circuit components as well as the circuit. Note: detecting defects is a step for using a functional blocks in an IC, hence the reliability data is based on past use.

35 U.S.C. 103(a) rejection of claim 12.

Balachandran teaches a fault detecting method for a semiconductor integrated circuit (see Abstract in Balachandran; Note: Balachandran teaches that test patterns are applied to an integrated circuit to detect faults used in generating various diagnostic lists), comprising: first detecting faults in a semiconductor integrated circuit to create a detection result (Step 230 in Figure 2 of Balachandran is a step for detecting faults in a

semiconductor integrated circuit to create a detection resultant vector); and combining said detection result with at least one of information about physical sites on a physical layout of the semiconductor integrated circuit to which said fault list corresponds where a possible fault is likely to occur and information required to reduce faults, to create a fault list (see Abstract and Figure 2 in Balachandran; Note: Balachandran teaches that a stuck-at-fault dictionary, i.e. a fault list, is provided to the test analysis tool so that the test analysis tool can prune the stuck-at-fault dictionary to construct intermediate and final pruned stuck-at-fault dictionaries referred to as initial diagnostic lists, composite dictionaries and final logical diagnostic list; Note also that Balachandran teaches that the stuck-at-fault dictionary comprises a plurality of nets of the circuit; col. 2, lines 56-60 and col. 6, lines15-20 in Balachandran teach that the system includes a physical database containing physical data for the physical layout of the circuit under test including geographical coordinates corresponding to the nets in the circuit and in particular corresponding to the nets in the stuck-at-fault dictionary, hence Balachandran teaches providing a stuck-at-fault dictionary fault list 100 in Figure 1 of Balachandran containing nets corresponding to information stored in a physical database 70 in Figure 1 identifying geographical coordinates, i.e., physical sites, on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur).

However Balachandran does not explicitly teach the specific use of detecting faults in said semiconductor integrated circuit by using the final fault list.

Rohrbaugh, in an analogous art, teaches the typical use of fault lists for compacting test vectors (see Figure 7 in Rohrbaugh). The Examiner asserts that Balachandran teaches

a method for creating a pruned fault list, which are typically used and required for designing tests, for creating test pattern sets and for testing for faults in Automatic Test Equipment (ATE) throughout the lifecycle of the DUT. Rohrbaugh, on the other hand teaches a typical use for generating test patterns from a fault list (see Figure 7 in Rohrbaugh) and using generated test patterns for testing a Device Under Test (DUT) by detecting faults using test patterns that were generated using a fault list, hence Rohrbaugh teaches detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Balachandran with the teachings of Rohrbaugh by including an additional step of detecting faults in said semiconductor integrated circuit by using the final fault list. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that detecting faults in said semiconductor integrated circuit by using the final fault list would have provided the opportunity to determine the integrity and fault-tolerance of a particular DUT during and after manufacture throughout the lifecycle of the DUT.

35 U.S.C. 103(a) rejection of claim 13.

Balachandran teaches omitting possible faults that having a specified low probability of occurrence from the fault list to define a remaining part of the fault list (col. 2, lines 43-48 in Balachandran).

35 U.S.C. 103(a) rejection of claim 14.

The Abstract in Balachandran states that the final logical diagnostic list is ranked in probabilistic order according to the probability of a fault; hence the fault list comprises data about a likelihood of a fault occurring at a physical site.

35 U.S.C. 103(a) rejection of claim 15.

Balachandran teaches the final logical diagnostic list is ranked in probabilistic order according to the probability of a fault; hence the fault list comprises data about a likelihood of a fault occurring at a physical site (see Abstract in Balachandran).

35 U.S.C. 103(a) rejection of claim 16.

Balachandran teaches weighting possible faults at physical sites according to their likelihood to achieve a specific fault coverage, thereby creating weighted possible faults (col. 6, lines 31-44 in Balachandran teach that if such a defect can cause a bridging fault between the two particular nets, the determination is weighted using the probability that a defect of that size exists to determine a final probability or ranking that particular bridging fault exists, hence ranking is a means for weighting in the Balachandran patent). Note: fault coverage is a probabilistic measure of detecting a set of faults in a semiconductor integrated circuit using a particular fault list.

35 U.S.C. 103(a) rejection of claim 17.

Col. 5, lines 22-42 in Balachandran teach that a composite dictionary including a listing of faults is used to create the final logical diagnostic list. A listing is an ordered set, i.e., the composite dictionary is ordered; hence Balachandran teaches arranging said possible faults an order in a composite dictionary before weighting said possible faults in the final logical diagnostic list.

35 U.S.C. 103(a) rejection of claim 20.

Defect data arranged in probabilistic order is reliability data giving a clear indication of the reliability of circuit components as well as the circuit. Note: detecting defects is a step for using a functional blocks in an IC, hence the reliability data is based on past use.

7. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran) and Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh) in view of Allan; Gerard Anthony (US 6066179 A).

35 U.S.C. 103(a) rejection of claims 7 and 18.

Balachandran and Rohrbaugh substantially teach the claimed invention described in claims 1-4 and 12-15 (as rejected above).

However Balachandran and Rohrbaugh do not explicitly teach the specific use of obtaining mask information from a layout device.

Allan, in an analogous art, teaches the susceptibility of an integrated circuit to defects is commonly obtained by a computer analysis of the integrated circuit mask layout (col. 1, lines 38-40 in Allen). The Examiner asserts that col. 2, lines 56-60 and col. 6, lines15-20 in Balachandran teach that the system in Balachandran includes a physical database containing physical data for the physical layout of the circuit under test including geographical coordinates corresponding to the nets in the circuit and in particular corresponding to the nets in the stuck-at-fault dictionary. The Examiner asserts that physical data for the integrated circuit mask layout is physical data for the physical layout of the circuit under test, hence use of physical data for the integrated circuit mask layout is a specific embodiment of the teachings in the Balachandran and Rohrbaugh patents.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Balachandran and Rohrbaugh with the teachings of Allan by including use of obtaining mask information from a layout device. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that obtaining mask information from a layout device would have provided the opportunity to impelement a specific embodiment of the teachings in the Balachandran and Rohrbaugh patents for which the Balachandran and Rohrbaugh patents were designed for.

8. Claims 10, 11, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran) and Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh) in view of Agrawal; Prathima et al. (US 5257268 A, hereafter referred to as Agrawal).

35 U.S.C. 103(a) rejection of claim 10, 11, 21 and 22.

Balachandran and Rohrbaugh substantially teaches the claimed invention described in claims 1-3, 5 and 6 (as rejected above). In addition, Balachandran and Rohrbaugh teach defining a required fault list by deleting from the fault list possible faults that are not required to achieve a specified fault coverage, in an order of unlikelihood of such possible faults, said specific fault coverage being a probability of detecting faults in the semiconductor integrated circuit to which said fault list corresponds (The Abstract in Balachandran states that the final logical diagnostic list is ranked in probabilistic order according to the probability of a fault; hence the fault list comprises data about a likelihood of a fault occurring at a physical site; col. 2, lines 43-48 in Balachandran teaches omitting possible faults that having a specified low probability of occurrence from the fault list to define a remaining part of the fault list); and detecting, according to said required fault list, remaining faults in such semiconductor integrated circuit (Rohrbaugh teaches a typical use for generating test patterns from a fault list in Figure 7 of Rohrbaugh and using generated test patterns for testing a DUT by detecting faults using test patterns that were generated using the fault list, hence Rohrbaugh teaches

detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list).

However Balachandran and Rohrbaugh do not explicitly teach the specific use of calculating fault coverage simultaneously with said detecting.

Agrawal, in an analogous art, teaches a step for detecting adequate fault coverage (See Steps 13 and 15 in Figure 1 of Agrawal).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Balachandran and Rohrbaugh with the teachings of Agrawal by including an additional step of use of calculating fault coverage simultaneously with said detecting. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of calculating fault coverage simultaneously with said detecting would have provided a measure of fault coverage.

Allowable Subject Matter

9. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133